SERIES SWITCH COMPATIBLE WITH CMOS TECHNOLOGY

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ABSTRACT — **Series switches with metal-to-metal contact have been fabricated to operate from DC to 40 GHz. Parylene is used as the structure material and polyamide as the sacrificial layer. The mechanical structure is of bridge type. The measured insertion loss is less than 0.5 dB from DC to 40 GHz, when switch is on. The isolation ranges from 40 dB at 2 GHz to 15 dB at 40 GHz, when the switch is off. A new way of planarizing circuit surface was presented.**

I. INTRODUCTION

Up till now, many types of MEMS switches have been introduced for RF/microwave circuits [1-7] and almost all of them require one or more layer of dielectric material, either for mechanical support or insulating material. Silicon oxide and silicon nitride are the most frequently used thin dielectric material for this purpose. Since the silicon oxide/nitride requires high temperature to grow or deposit, the switch has to be integrated with transistors in a hybrid MMIC form to avoid potential damage caused by the thermal cycle. This increases cost and limits the number of circuits on a single chip. In this paper, a new type of MEMS switch has been presented. This switch (Fig.1) has been fabricated with parylene serving as structure material and polyamide as sacrificial layer. The whole process can be implemented at low temperature (the highest thermal cycle is 30 min 150 °C baking) with transistor such as CMOS or HBT.

The finished switch is shown in Fig.1A. The bridge with length around 950 μm is suspended 2.5 μm above the substrate. The deflection from that level is of the order of a fraction of a micron. Meander connection beam (shown in the Fig. 1B) is introduced as two supporting beams to enhance their ability of stretching and to reduce stress generated in the beam during releasing. Two actuation pads (200μm X 200μm) are fabricated on the bridge. Another pair of actuation pad is on the circuit. When DC bias applied between the pads on the bridge and on the circuit, the switch is pulled down. As shown in Fig. 1C, the switch is very flat when fully released due to low build in stress. The metal is underneath the parylene beam at the RF contact.

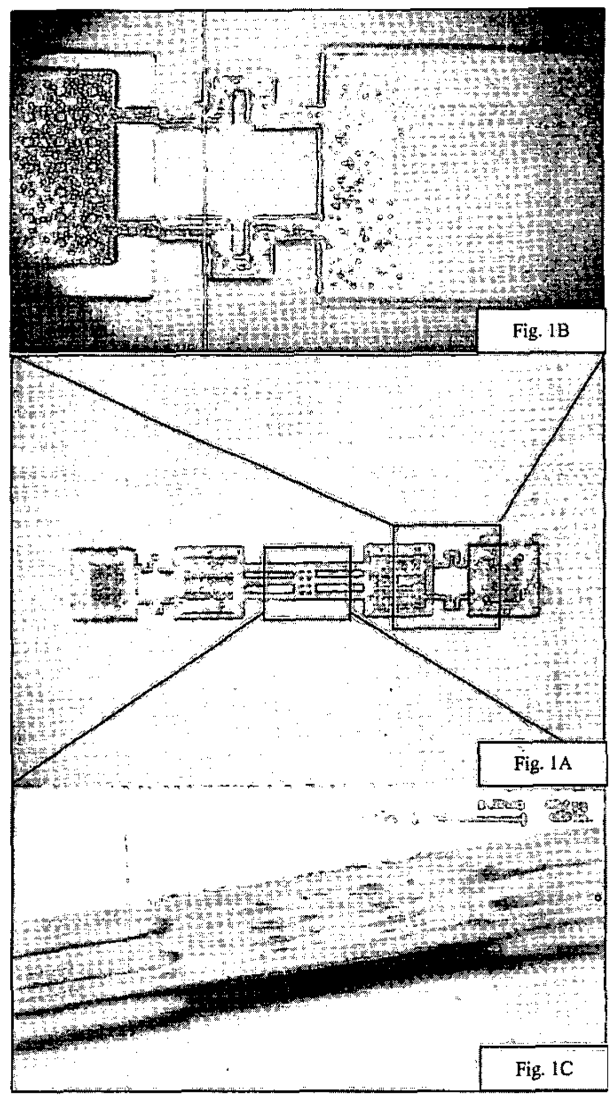


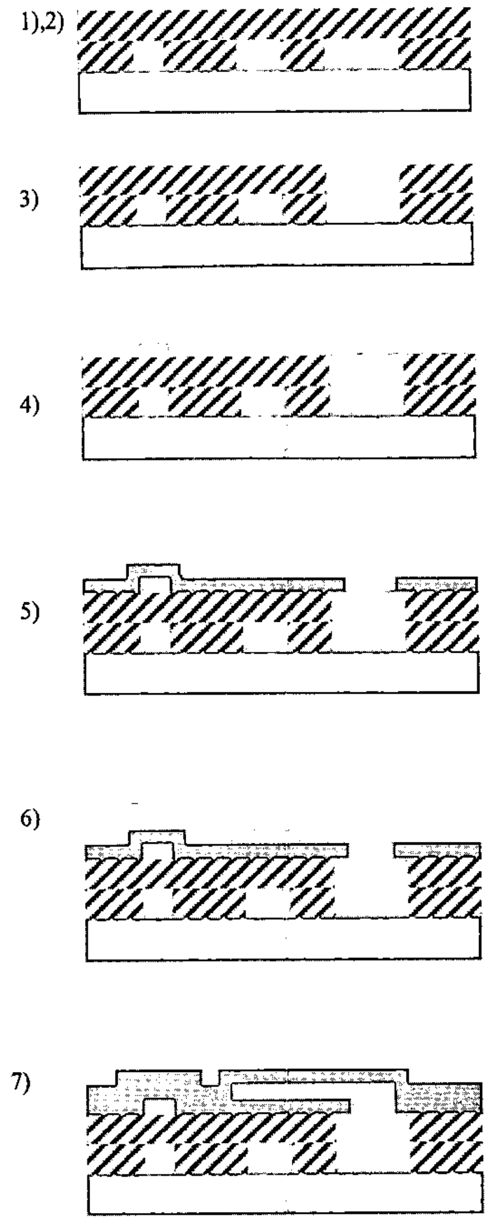
Fig.1A Series switch with bridge structure. 1B Enlarged beam section. 1C Enlarged RF contact.

II. DESGIN AND FABRICATION

Parylene is a commercially available polymer used as a protective PCB coating. Its special properties[8] make it a ideal material for MEMS switch: 1) The parylene can be deposited at room temperature; 2) It can form very thin layers. For parylene as thin as 0.1 μm, the DC breakdown voltage is as high as 800 V. For 3 μm thick, it can sustain 2000 V; 3) It resist room temperature chemical attack and are insoluble in all organic solvent up to 150 °C; 4) It has low Young's modulus (around 2.5 GPa), large elongation to break (200%) and low density (1.29 g/cm^3); 5) It is truly conformal and pinhole free at thickness down to 0.4 μm. Due to the above reasons, the parylene is chosen as the switch material. The final structure has low stress and is flat and self-supportive.

The switch has been designed to be a metal-to-metal contact series switch. We have designed the switch in a bridge form as shown in Fig 1. The pull-in voltage varies to be 10-20V, depending upon the thickness and length of the beam. CPW line is used as the transmission line. The CPW line has dimensions of (S/W/S = 40/60/40μm) chosen for the 50 Ω at 30 GHz. The processing procedure as shown in figures consists of the following steps:

1) Deposit Au as circuit layer and planarize the surface. We found out that during the RF circuit metalization, usually 8000-9000 Å Au layer will cause a hilly profile for the sacrificially layer and will warp the structure deposited on it. So we developed a method [9] (US patent pending, UM 2112) to planarize the surface. 2) Apply polyamide onto the chip as sacrificial layer. Bake at 150 °C for 30 min. This is the only thermal process in this fabrication. After baking, the polyamide is 2.5 μm thick. 3) RIE etch the sacrificial layer and deposit Au to form the anchor. 4) Deposit Au and lift-off to make the RF contact which is 8000 Å thick. 5) Deposit 0.5 μm parylene. 6) Deposit and lift-off to make the inner beam for electro-actuation. 7) Deposit 2.5 μm parylene and RIE to define the bridge. 8) Remove the sacrificial layer. 9) Release the structure with Critical point drying. The diagram shows one half of the bridge.



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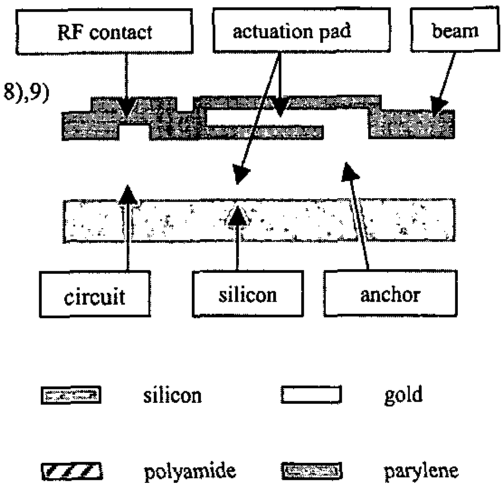

Fig 2. Diagram of the process.

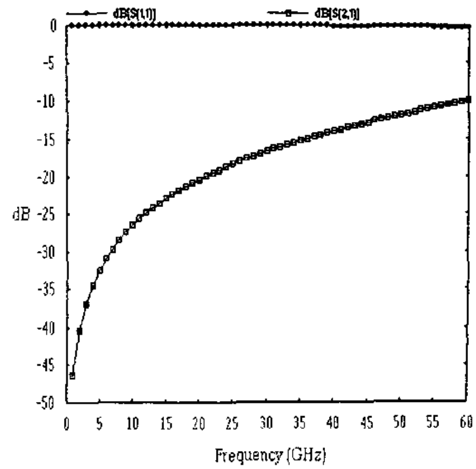

Fig.3 Simulated return loss and isolation when switch is off (up state).

III. Simulation and Measurement

The Zeland IE3D simulated results are shown in Fig 3. and Fig. 4. The switch has a calculated isolation of 50 dB (at DC) to 15 dB (at 40 GHz) when is off, and 0 dB insertion loss when is in on state since the simulation includes zero losses.

The measurements are based on an on-wafer TRL calibration. The isolation ranges from 50 dB at 2 GHz to 15 dB at 40 GHz, when the switch is in off state (Fig. 5). When the switch is in the on state, the insertion loss has been measured to be 0.5 dB at from DC to 40 GHz (Fig. 6). There are some discrepancies between the simulation and the measured results because of this measured loss. The loss is partially due to the SiO_2 left on the silicon wafer to avoid possible Schottky barriers between the circuit layer and the Si substrate. It is found out in experiment that this loss associated with silicon oxide is higher than that of Si. In the future design, the dielectric material on substrate between signal line and finite ground line of the CPW line will be removed. The bottom of the RF contact is coated with chromium and it incurs loss higher than Au. Also when two metals (Au and Cr) contact each other, the difference in work function causes higher loss than contact between just Au. In the future, the chromium will be removed too.

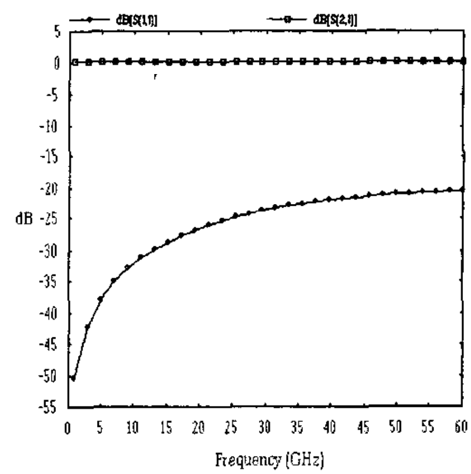

Fig.4 Simulated return loss and insertion loss when switch is on (down state).

V. Conclusion

A new type of series switch has been presented. A polymer called Parylene is used as the structure material. The whole process only requires one step of thermal treatment, which is 150 °C for 30 min. This renders it easily to be fabricated with transistors without worry about the dopant diffusion caused by the heating. The structure is very robust, even intentional damage by probes is impossible. A new method to planarize the circuit surface is developed. Detailed results and discussion will be presented at the conference.

Acknowledgement

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References

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[9] US patent pending, UM 2112. Yongming Cai and Linda Katehi, April, 2001.

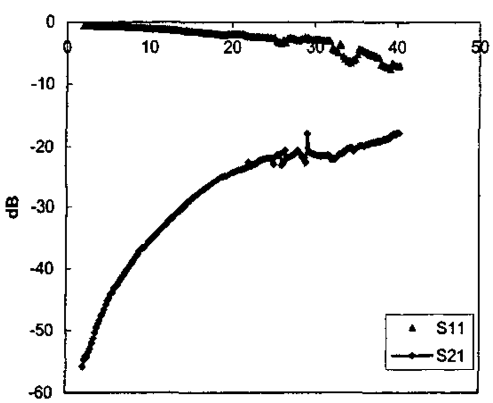

Fig.5 Measured return loss and isolation loss when switch is off (up state)

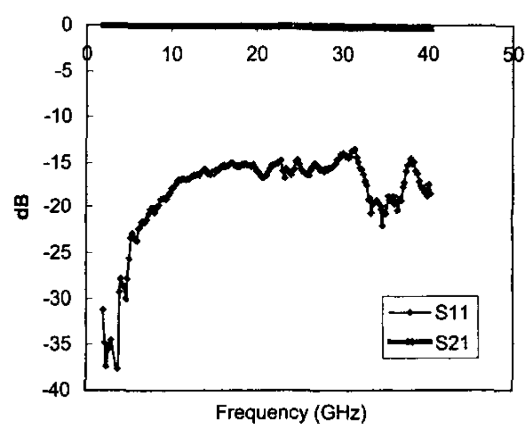

Fig.6 Measured return loss and insertion loss when switch is on (down state)